Features

- **HMP8156 video encoder**

- **HMP8112/8112A video decoder**

- **Analog input formats**
  - **Composite (up to four inputs)**
  - **Y/C (S-Video)**
  - **Analog RGB with sync**

- **Digital parallel BT.656 input**

- **Analog output formats**
  - **Y/C + two composite**
  - **RGB + composite (SCART)**

- **NTSC and PAL operation**

- **ITU-R BT.601 and square pixel operation**

- **Three Megabyte video RAM on board**

- **Programmable sync generator**

- **Analog sync separator**

- **User selectable hue, saturation, contrast and brightness controls**

- **Closed captioning insertion**

- **Windows95™ application program**

Applications

- **Video image capture and display**

- **Real time standards conversion**

- **Live color editing**

Description

The HMP8156EVAL2 Video Evaluation Platform is a PC ISA Bus add-in card designed to demonstrate the capabilities and performance of the HMP8156 NTSC/PAL Encoder and the HMP8112 NTSC/PAL Decoder.

The board has three input data paths: analog composite via the HMP8112 analog component RGB via a Intersil A/D design, and digital BT.656. For all three input paths, the board outputs analog video via the HMP8156. The board can output one composite video signal and either S-Video and a second composite signal, or component RGB video.
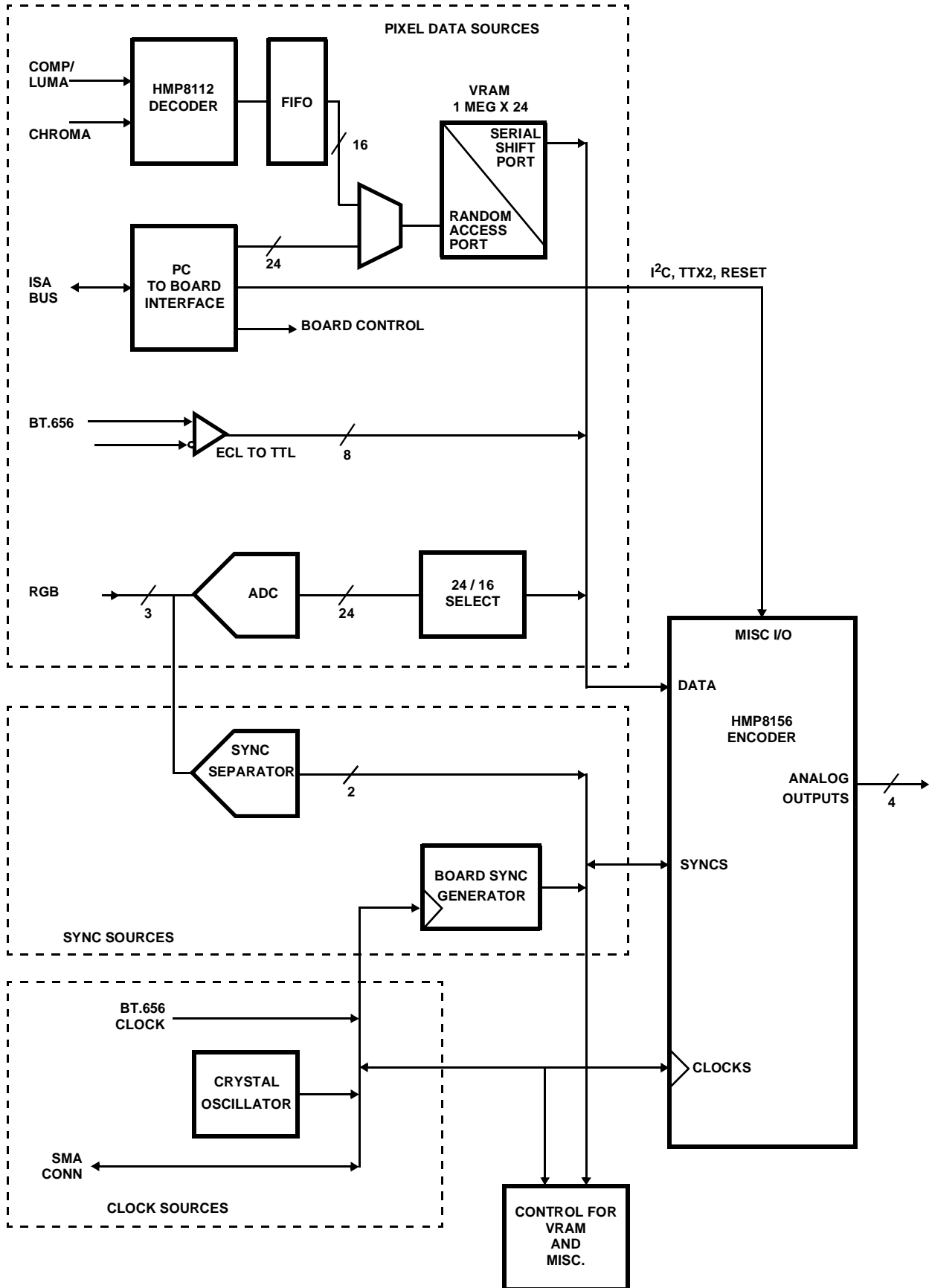
The board accepts analog composite or S-video in NTSC or PAL format. The decoder converts the analog signal into digital data and stores it in the three megabyte video frame buffer. The encoder reads the data from the video RAM and generates analog video in NTSC or PAL format. The encoder generates its own timing information, or it may be driven by the on board programmable sync generator. The input and output formats may be different, eg: NTSC input and PAL output.

The board accepts analog RGB video with composite sync. Three high-performance ADCs convert the analog signals to digital data and drive the encoder. A sync separator derives timing information for the encoder from the input. The encoder converts the digital data and timing information into analog video in the same format as the input video.
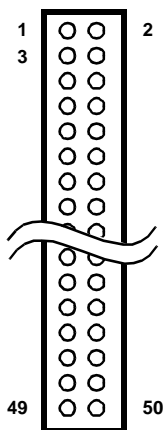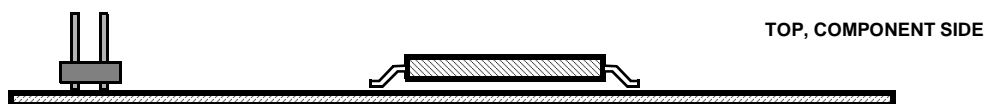
The board accepts a digital parallel BT.656 data stream. Translators convert the ECL input to TTL levels and drive the encoder. The encoder converts the data and its embedded timing information into analog video.

The user interface to the evaluation platform is an easy to use Windows95 application program. The application provides host control to program the board. It provides user access to all of the decoder and encoder operating parameters and also allows the user to load (store) video images in the video RAM from (to) the PC file system.

Functional Block Diagram

PIXEL DATA SOURCES

COMP/
LUMA

CHROMA

HMP8112
DECODER

FIFO

16

VRAM
1 MEG X 24

SERIAL
SHIFT
PORT

RANDOM
ACCESS
PORT

24

PC
TO BOARD
INTERFACE

ISA
BUS

BOARD CONTROL

I²C, TTX2, RESET

BT.656

ECL TO TTL

8

RGB

ADC

3

24

24 / 16
SELECT

MISC I/O

DATA

HMP8156
ENCODER

ANALOG
OUTPUTS

4

SYNC
SEPARATOR

2

BOARD SYNC
GENERATOR

SYNCS

SYNC SOURCES

BT.656
CLOCK

CRYSTAL
OSCILLATOR

CLOCKS

SMA
CONN

CLOCK SOURCES

CONTROL FOR
VRAM
AND
MISC.

Flywire Physical Interface

TOP, COMPONENT SIDE

TOP VIEW

50 POSITION HEADER,
0.025 INCH SQUARE POSTS,
0.100 INCH SPACING

CONNECTOR PINOUTS

SIGNAL	PIN
VCC	1
GND	2
N/C	3
N/C	4
PIX<23>	5
PIX<22>	6
PIX<21>	7
PIX<20>	8
PIX<19>	9
PIX<18>	10
PIX<17>	11
PIX<16>	12
GND	13
VCC	14
PIX<15>	15
PIX<14>	16
PIX<13>	17

SIGNAL	PIN
PIX<12>	18
PIX<11>	19
PIX<10>	20
PIX<9>	21
PIX<8>	22
-VSYNC_ENC	23
GND	24
VCC	25
VCC	26
GND	27
-HSYNC_ENC	28
PIX<7>	29
PIX<6>	30
PIX<5>	31
PIX<4>	32
PIX<3>	33
PIX<2>	34

SIGNAL	PIN
PIX<1>	35
PIX<0>	36
VCC	37
GND	38
FIELD_ENC	39
-BLANK_ENC	40
N/C	41
N/C	42
SCLK	43
SDATA	44
N/C	45
-RESET_A	46
PIXCLK_RDH	47
VIDCLK	48
GND	49
VCC	50

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